# Reducing the level shift and three phase ac current rise at the movement of turning on

S.DEVI LAVANYA[1], Dr. KIRUBAKARAN.D[2]

**ABSTRACT-** This paper presents a multilevel inverter that consists of a standard 3-leg two level inverter cascaded with two new neutral point clamped H-bridge inverter. The paper is concentrated to reduce the initial current and voltage rise at the movement of turning on and to reduce the level shit this is achieved by using a new PWM technique. The control signals for this multilevel inverter is obtained by using carrier based PWM technique. The proposed paper is used to obtain a three phase ac power generation making it suitable for industries which is verified using MATLAB/SIMULINK software. The results of the simulated output waveform of three phase voltage and phase current is obtained using MATLAB/SIMULINK software. The new NPC flying capacitor H-Bridge inverter and a new PWM technique is used in this paper.

**KEYWORDS-** Two NPC H-bridge, PWM technique, multilevel inverter, two level flying capacitor inverter, sinusoidal waveform, three phase ac power generation, Industries.

## 1. INTRODUCTION

A multilevel inverter is a power electronic converter built to synthesize a desired AC voltage from several levels of dc voltages in which the DC levels are obtained from batteries, solar cells, capacitors, etc. In this paper, the proposed topology used to reduce the initial current rise at the movement of turning on. The proposed topology uses a new PWM technique because of which the initial current rise at the movement of turning on is reduced almost nil. The proposed topology also shows the comparison between other topologies that is when we use the other PWM techniques there is a level shift when we approach sine wave which does not take place in the proposed topology. A three phase AC current and voltage generation is obtained in the proposed topology which makes it suitable for industries. The prototype is tested with capacitive type of load the output of which can be connected to any type of three phase AC load especially induction motor since the output obtained is three phase AC sinusoidal wave form. This analysis is carried out using MATLAB/SIMULINK software. Several topologies and Several PWM techniques were carried out to obtain sinusoidal waveform or to increase the number of levels. The proposed topology implements a simple carrier based PWM technique and uses a new two NPC H-bridge inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require various pulse width modulation (PWM) strategies, which increase the switching frequency of the power devices. In the case of multilevel inverters, as the number of voltage levels increases the harmonic content of the output voltage waveform decreases, even without using any pulse width modulation technique. As the switching frequency is reduced the power losses are also minimized, and thereby increasing the efficiency of the system. The paper is focused to reduce the initial current rise at the movement of turning on and also there is no any level shift at the output wave form which takes place when we approach it to obtain a sinusoidal waveform this happens when we use other PWM technique especially when the carrier is ramp wave or level shifted carrier. The proposed topology uses triangular wave as carrier and all the carriers operate at same frequencies and different amplitude the frequency of the carrier used is around 1 kHz. The proposed topology uses a two level inverter cascaded with new neutral point clamped H-Bridge. This is the recent trend in multilevel inverter developed by this proposed topology. Further investigations are not required for multilevel inverter to increase the number of levels. The proposed topology implements the development of three phase sinusoidal AC voltage and current waveform which is obtained using a single DC voltage source at desired output voltage and frequency by using a power electronics device that is called an inverter. In future the solar cells can be used as dc source.

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## 2. DESIGN OF THE PROPOSED TOPOLOGY

The input given to the two level inverter is $V_{dc}$ and the input given to the first H-bridge inverter is $V_{dc}/4$ and the input given to the second H-bridge inverter is $V_{dc}/8$ the input to the H-bridges given is by means of capacitor charging and discharging of capacitor of value 12 farads. The value of the output capacitor used is 20 farads. The dc supply can be obtained using solar panels as dc source. In future the three phase ac supply can be obtained using solar panels as dc source. The input dc voltage given can be of any value.

## 3. PWM TECHNIQUE

The PWM technique used in this topology is carrier based PWM technique which uses a sine wave as a reference wave and triangular wave as carrier without level shift. The triangular wave is used as a carrier as shown in the proposed PWM technique.

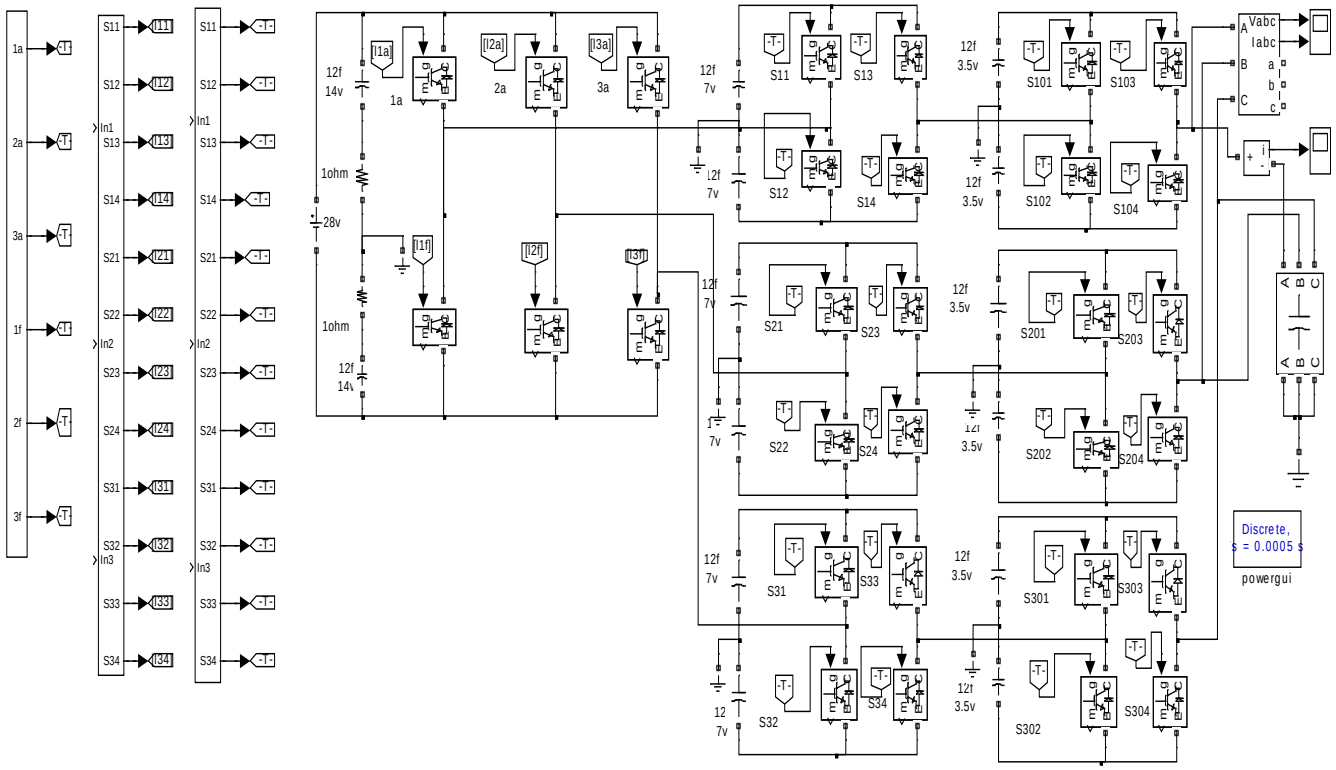


FIGURE.1. SIMULINK/MATLAB CIRCUIT FOR PROPOSED THREE-PHASE MULTILEVEL INVERTER WITH TWO NPC H-BRIDGE INVERTER

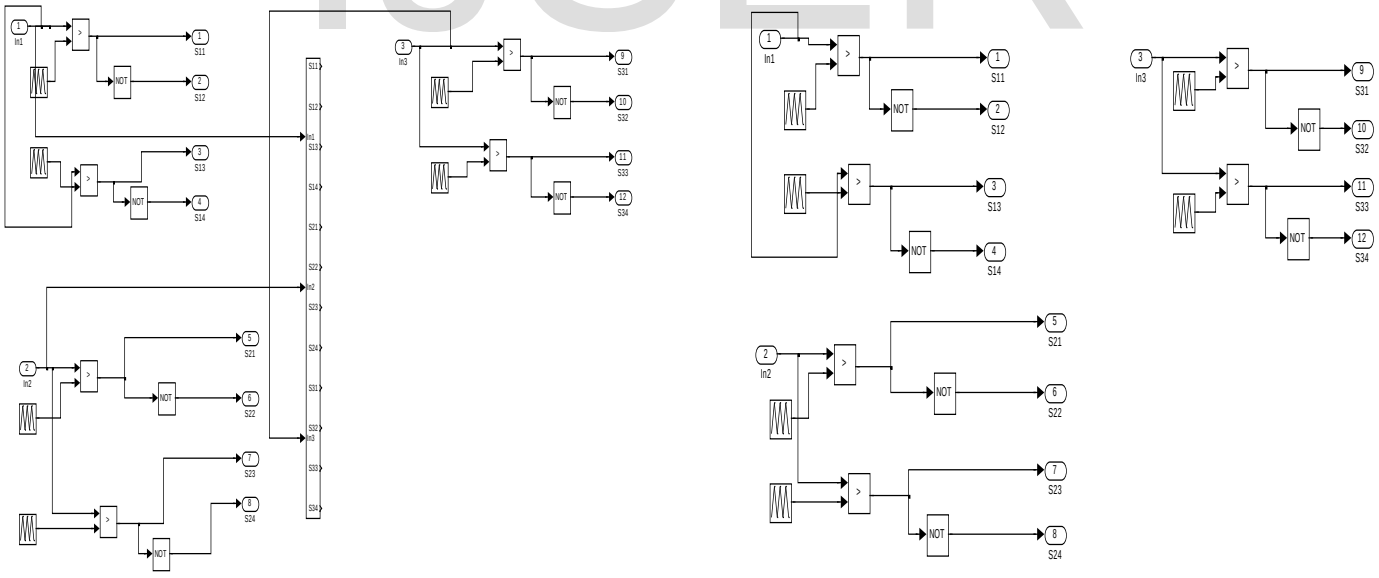

FIGURE.2. THE PWM SIGNALS GIVEN TO NPC H-BRIDGE INVERTER 1 AND H-BRIDGE INVERTER 2

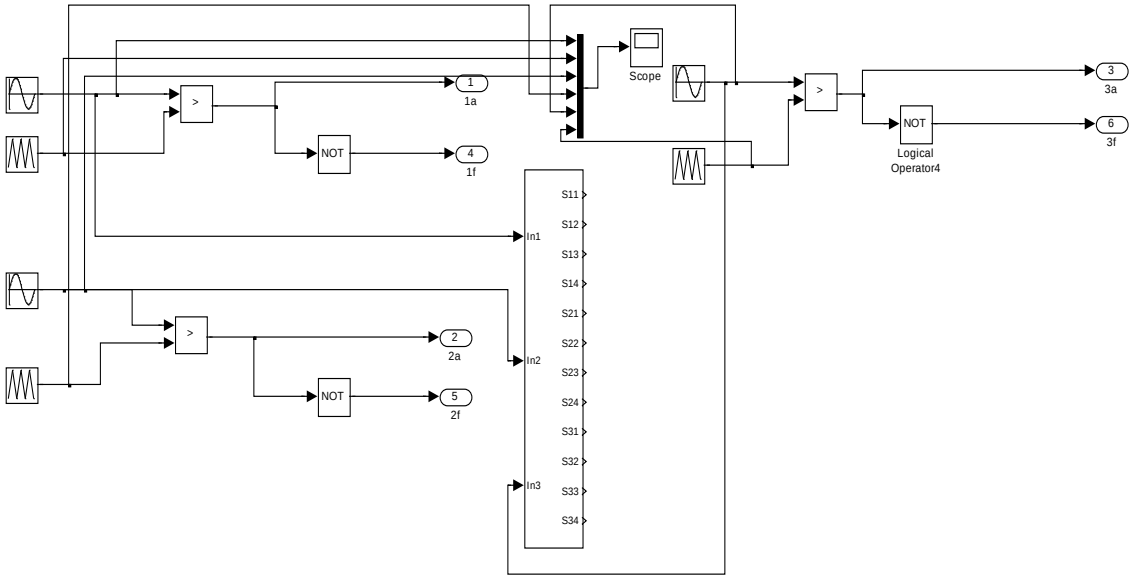


FIGURE.3. THE PWM SIGNALS GIVEN TO TWO LEVEL INVERTER.

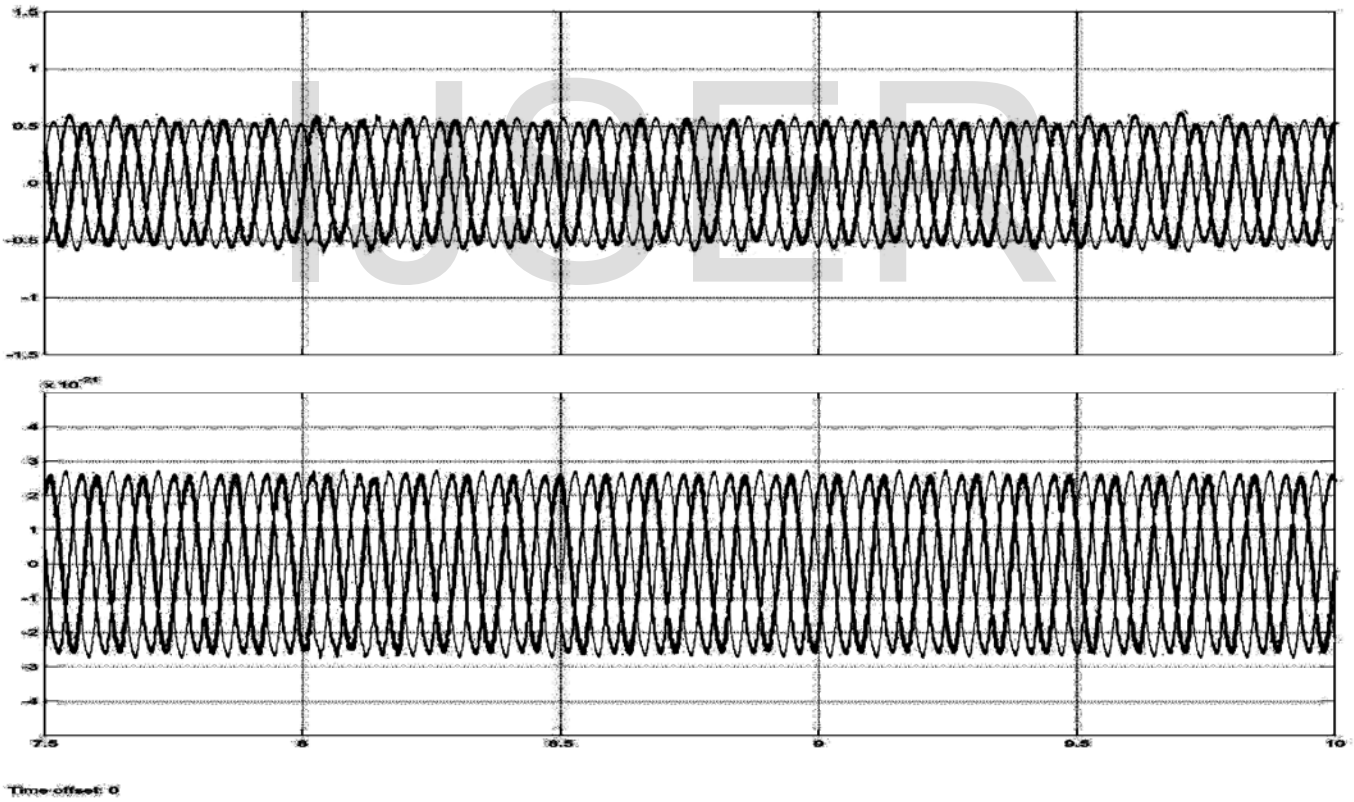


FIGURE.4. THREE PHASE OUTPUT CURRENT AND VOLTAGE WAVEFORM OF THE PROPOSED TOPOLOGY.

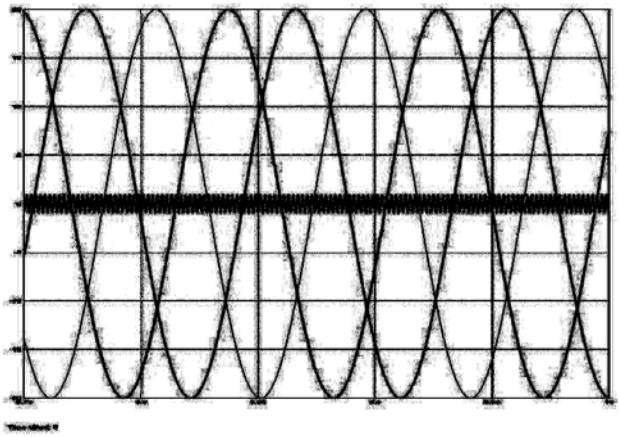

FIGURE.5. THE PWM INPUT SIGNALS.

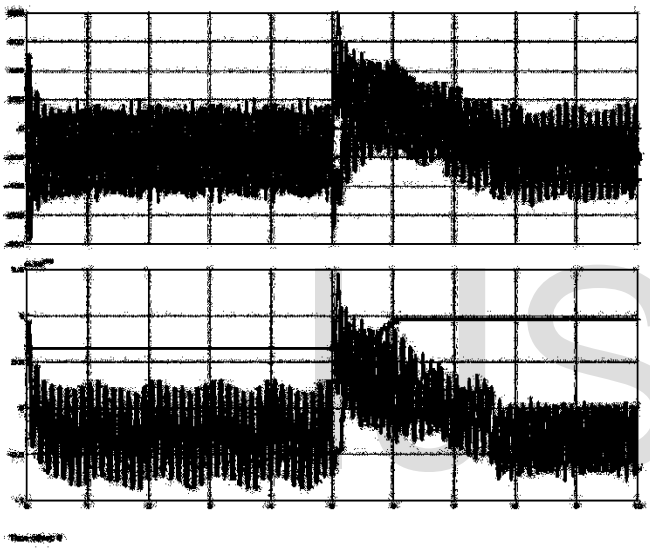

FIGURE.6. THE OUTPUT OF OTHER TOPOLOGIES

## 4. COMPARISON WITH OTHER TOPOLOGIES

Figure (6) shows the comparison with other topologies when we use other PWM techniques example when the carrier is ramp wave there is a level shift when we approach a sinusoidal waveform but the proposed topology implements a new PWM technique where there is no level shift and also the initial current rise is limited at the movement of turning on the output of which is shown in figure (7). When we use other PWM techniques such as when the carrier is level shifted or if the carrier is ramp wave there is an occurrence of level shift as shown in figure(6). The PWM technique used in the proposed topology is of the form as shown in figure (5). Since the proposed topology uses NPC H-bridge inverter it reduces the number of components.

As per paper (11) and paper (2) there is a common mode voltage problem when we use carrier based PWM technique but in the proposed topology such thing does not take place. As per paper (1) SVPWM to obtain a sinusoidal waveform it should be operated in over modulation region but the proposed topology uses a simple PWM technique to obtain sinusoidal waveform with less number of components compared to paper (2).

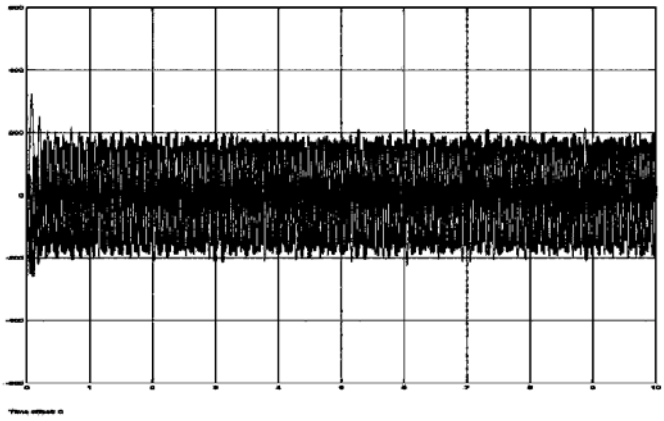

FIGURE.7. OUTPUT OF PROPOSED TOPOLOGY

## 5. CONCLUSION

When we use the proposed topology there is no level shift problem and also there is no initial current rise at the movement of turning on which is verified using MATLAB/SIMULINK software using a suitable PWM technique. The proposed topology reduces the number of components compared to other topologies the reason is that here we have used a new NPC H-bridge inverter. Figure.7. shows the output of the proposed topology there is no level shift or there is no any initial current rise.

## REFERENCES

[1] A General Space Vector PWM Algorithm for Multilevel Inverters, Including Operation in Overmodulation Range Amit Kumar Gupta, *Student Member*, *IEEE*, and Ashwin M. Khambadkone, *Senior Member*, *IEEE* TRANSACTIONS ON POWER ELECTRONICS, VOL. 22, NO. 2, MARCH 2007.

[2] A.V.RAVI KUMAR, G.RAVI KUMAR International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 2,Mar-Apr 2012, pp.1619-1626 1619 | P a g e Comparison of Multi-level inverters by reducing common mode voltages and DC-link capacitor voltage balancing for IM drives.

[3] P. J. Link, "Minimizing electric bearing currents in ASD systems," *IEEE Ind. Applicat. Mag.*, vol. 5, pp. 55–66, July/Aug. 1999.

[4] D. Rendusara, E. Cengelci, P. Enjeti, V. Stefanovic, and W. Gray, "Analysis of common mode voltage -"Neutral shift "in medium voltagePWM adjustable speed drive (MV-ASD) systems," in *Proc. IEEE PESC'99*, 1999, CD-ROM.

[5] L. Palma, L. Morán, and R. Wallace, "A simple and cost effective solution to reduce motor bearing currents in PWM inverter drives," in *Proc. ISIE 2000*, pp. 425–429.
[6] H. Zhang, A. von Jouanne, and A. Wallace, "Multilevel inverter modulation schemes to
eliminate common-mode voltages," in *Conf. Rec.IEEE-IAS Annu. Meeting*, 1998, CD-ROM.
[7] International Journal of Engineering and Technology Volume 2 No. 7, July, 2012 ISSN: 2049-3444 © 2012 – IJET Publications UK. All rights reserved. 1131 Investigations on Three PhaseFive Level Flying Capacitor Multilevel
Inverter R.Balamurugan1, S.P.Natarajan2, R.Bensraj3.
[8] M. Venu Madhav " MATLAB based Analysis and Simulation of Multilevel Inverters" International Journal of
Computer Applications (0975 – 8887) Volume 39– No.4, February 2012.
[9]. R.S. Kanchan, M.R. Baiju, K.K. Mohapatra, P.P. Ouseph and K. Gopakumar "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages"
[10] International Conference on Emerging Frontiers in Technology for Rural Area (EFITRA) 2012 Proceedings published in International Journal of Computer Applications® (IJCA) "Performance of Sinusoidal Pulse Width
Modulation based Three Phase Inverter". Pranay S. Shete.
[11] Comparisons of Space-Vector Modulation and
Carrier-Based Modulation of Multilevel Inverter Wenxi Yao, Haibing Hu, and Zhengyu Lu, *Senior Member*, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 23, NO. 1, JANUARY 2008.



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